412 Rec'd PCT/PTO 10 MAR 2000

FORM PTO-1390 (REV. 5-93)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEY'S DOCKET NUMBER 67190/978621
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/508396

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATES CLAIMED
PCT/DE98/02692	(4.09.98) 4 September 1998	(10.09.97) 10 September 1997

TITLE OF INVENTION
METHOD AND CONFIGURATION FOR TESTING DIGITAL PROTECTION DEVICES

APPLICANT(S) FOR DO/EO/US
KAISER, Steffen and WINTER, Wilhelm

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) immediately rather than delay applicable time limit set in 35 U.S.C. examination until the expiration of the 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S C 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1 98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☐ A **FIRST** preliminary amendment.
    ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

Express Mail No.:

EL179105382 US

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U.S. APPLICATION NO. (If known, see 37 C.F.R. 1.5) 09/508396	INTERNATIONAL APPLICATION NO. PCT/DE98/02692	ATTORNEY'S DOCKET NUMBER 67190/978621

17. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)-(5)):

Search Report has been prepared by the EPO or JPO ... $840.00
International preliminary examination fee paid to USPTO (37 CFR 1.482) ... $670.00
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) ... $760.00
Neither international preliminary examination fee (37 CFR 1 482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO ... $970.00
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ... $96.00

	CALCULATIONS	PTO USE ONLY
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	7 - 20 =	0	X $18.00	$ 0	
Independent Claims	2 - 3 =	0	X $78.00	$ 0	
Multiple dependent claim(s) (if applicable)			+ $260.00	$	

TOTAL OF ABOVE CALCULATIONS =	$ 840	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28).	$	
SUBTOTAL =	$ 840	
Processing fee of $130.00 for furnishing the English translation later the ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +	$	
TOTAL NATIONAL FEE =	$ 840	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +	$	
TOTAL FEES ENCLOSED =	$ 840	
	Amount to be: refunded	$
	charged	$

a. ☐ A check in the amount of $_____ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. 11-0600 in the amount of **$840.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to 11-0600. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) Deposit Account No. or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Kenyon & Kenyon
One Broadway
New York, New York 10004

by Richard L. Mayer (Reg No 22,490)
SIGNATURE

Richard L. Mayer, Reg. No. 22,490
NAME

10 March 2000
DATE

264290

[67190/978621]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s)	:	Steffen KAISER et al.
Serial No.	:	09/508,396
Filed	:	March 10, 2000
For	:	METHOD AND ARRANGEMENT FOR TESTING DIGITAL PROTECTIVE CIRCUITS
Examiner	:	To Be Assigned
Art Unit	:	To Be Assigned

Assistant Commissioner
for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT AND
37 C.F.R. § 1.125 SUBSTITUTE SPECIFICATION STATEMENT

SIR:

Please amend the above-identified application before examination, as set forth below.

IN THE SPECIFICATION AND ABSTRACT:

In accordance with 37 C.F.R. § 1.121(b)(3), a Substitute Specification (including the Abstract, but without claims) accompanies this response. It is respectfully requested that the Substitute Specification (including Abstract) be entered to replace the Specification of record.

IN THE CLAIMS:

On the first page of the claims, first line, change "What is claimed is:" to: --What Is Claimed Is:--.

IN THE DRAWINGS:

Please amend the drawings as indicated on the attached red-marked sheet.

EL244506391US

IN THE CLAIMS:

Please cancel, without prejudice, claims 1-7 in the underlying PCT application. Please also cancel, without prejudice, claims 1-7 in the annex to the International Preliminary Examination Report ("IPER").

Please add the following new claims:

8. (New) A method for testing a digital protective circuit, comprising:

outputting digital current and voltage signals in cycles by a data processor to simulate a current and voltage response of a power supply network;

buffering consecutively the output digital current and voltage signals;

upon reaching a specific quantity of buffered digital current and voltage signals, outputting oldest ones of the buffered digital current and voltage signals in cycles;

rebuffering newer ones of the digital current and voltage signals;

generating corresponding currents and voltages from the output oldest ones of the digital current and voltage signals;

supplying the corresponding currents and voltages to the protective circuit;

detecting tripping signals from the protective circuit;

upon an occurrence of a tripping signal, outputting by the data processor network error-specific digital current and voltage signals while the oldest ones of the digital current and voltage signals continue to be output in cycles; and

buffering the output network error-specific digital current and voltage signals.

9. (New) The method according to claim 8, further comprising:

determining the specific quantity of digital current and voltage signals buffered as a function of a response time of switches for which the protective circuit is used, taking a cycle time into account.

10. (New) The method according to claim 8, wherein the buffered digital current and voltage signals are output at an interval that corresponds to a duration of a tripping signal-free test period needed to output further buffered digital current and voltage signals.

11. (New) The method according to claim 8, wherein the buffered digital current and voltage signals are output at an interval that is greater than a duration of a tripping signal-free test period needed to output further buffered digital current and voltage signals.

12. (New) An arrangement for testing a digital protective circuit, comprising:

a data processing system to simulate a current and voltage response of a power network using a network model by outputting digital current and voltage signals in cycles;

a buffer assigned to the data processing system in which the output digital current and voltage signals are buffered consecutively, wherein, upon reaching a specific quantity of buffered digital current and voltage signals, oldest ones of the buffered digital current and voltage signals are output in cycles, newer ones of the buffered digital current and voltage signals being rebuffered;

a converter unit located downstream from the data processing system, the converter unit to generate corresponding currents and voltages from the output oldest ones of the digital current and voltage signals and to supply the corresponding currents and voltages to the protected circuit; and

a sensing arrangement assigned to the protective circuit, the sensing arrangement triggering the data processing arrangement to output network error-specific digital current and voltage signal from the protective circuit.

13. (New) The arrangement according to claim 11, wherein the buffer is sized to buffer all digital current and voltage signals output during a tripping signal-free test period corresponding to a response time of switches provided for interaction with the protective circuit.

14. (New) The arrangement according to claim 11, wherein the buffer is a ring buffer.

Remarks

The Preliminary Amendment cancels, without prejudice, claims 1-7 in the underlying PCT application. This Preliminary Amendment further cancels, without prejudice, claims 1-7 in the annex to the IPER, and adds new claims 8-14. The new claims conform the claims to U.S. Patent and Trademark Office rules and do not add new matter.

The above amendments to the title, specification and abstract conform the title, specification and abstract to U.S. Patent and Trademark Office rules, and do not introduce new matter into the application.

The underlying PCT application No. PCT/DE98/02692 includes an International Search Report dated February 19, 1999. An English translation of the Search Report is included herewith.

The underlying PCT application also includes an IPER, dated December 7, 1999. An English translation of the IPER and the annex thereto is included herewith.

It is respectfully submitted that the subject matter of the present application is new, non-obvious, and useful. Prompt consideration and allowance of the application are respectfully requested.

Respectfully submitted,

Dated: 25 July 2001

By: _____

Richard L. Mayer
Reg. No. 22,490

KENYON & KENYON
One Broadway
New York, NY 10004
(212) 425-7200

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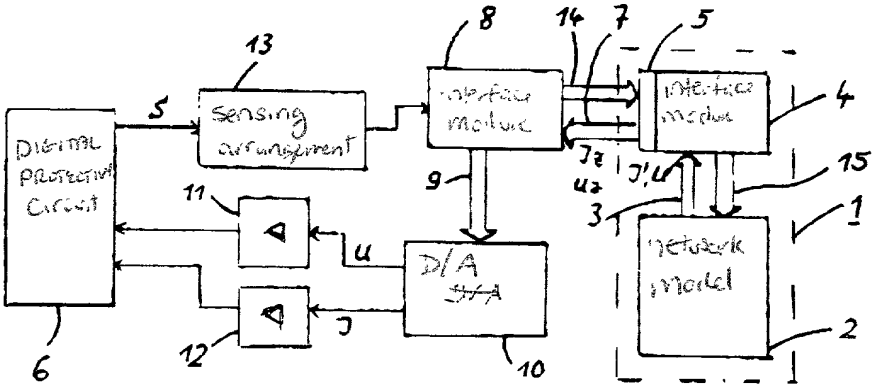
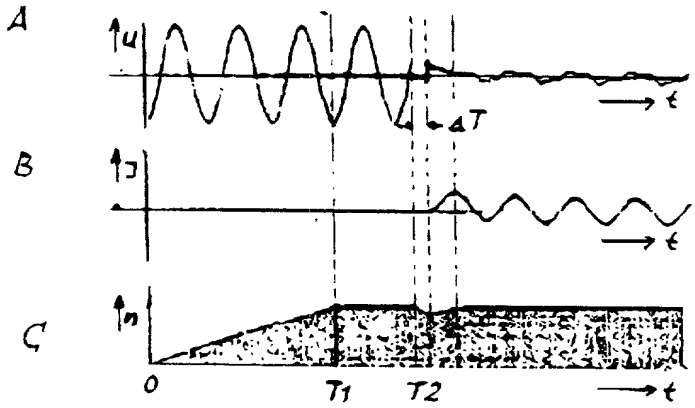

Digital protective circuit
Sensing arrangement
Interface module
Interface module
Network model
D/A
u
J
8
14
7
5
13
4
15
1
2
3
9
11
12
10
6

Fig 1


A
B
C
u
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n
t
ΔT
0
T1
T2

Fig 2

09/508396

#11

[67190/978621]

METHOD AND ARRANGEMENT FOR TESTING DIGITAL PROTECTIVE CIRCUITS

FIELD OF THE INVENTION

The present invention relates to a method for testing digital protective circuits in which data processing means are used to simulate the current and voltage response of a power supply network by outputting digital current and voltage signals in cycles; corresponding currents and voltages are generated from the digital current and voltage signals and supplied to a protective circuit to be tested; and tripping signals from the respective protective circuit are detected.

BACKGROUND INFORMATION

A method of this type is described in "Elektrizitätswirtschaft", Vol. 78 (1979), No. 1, pages 18 to 23. In this method, a data processing system emits digital current and voltage signals in cycles on the basis of the current and voltage ratios present in a power supply network; the data processing system thus forms a network model. Corresponding currents and voltages can be generated from the digital current and voltage signals and supplied to a protective circuit to be tested. When currents and voltages corresponding to an error in the simulated power supply network are applied to the protective circuit to be tested, the latter generates a tripping signal. The occurrence of the tripping signal can be assigned to the respective currents and voltages to draw conclusions about the tripping performance of the respective protective circuit to be tested.

To test the digital protective circuits under conditions that are as close to reality as possible, it is useful to control the data processing system simulating the power supply network and representing a network model when detecting a tripping signal so that the data processing system also outputs network error-specific digital current and voltage signals. Because this requires longer computing times than are needed for

digital current and voltage signals that indicate a normal, continuous variation of currents and voltages, it is possible to use a very high-speed data processing system and to have the latter output network error-specific digital current and voltage signals when a tripping signal is emitted by the respective protective circuit to be tested. However, a data processing system of this type is highly complex and therefore very expensive to produce or purchase.

SUMMARY

An object of the present invention is to provide a method for testing digital protective circuits in which a conventional data processing system, such as a personal computer, can be used to test digital protective circuits under close-to-real conditions even using network error-specific digital current and voltage signals from a data processing system of this type.

This object is achieved with a method according to the present invention in that when the test of a protective circuit begins, the output digital current and voltage signals are first buffered consecutively, and, upon reaching a specific quantity of buffered digital current and voltage signals, the oldest buffered digital current and voltage signals in each case are output in cycles and supplied to the respective protective circuit to be tested, and more recent output digital current and voltage signals are rebuffered; upon the occurrence of a tripping signal, a data processing arrangement outputs network error-specific digital current and voltage signals, while the oldest buffered digital current and voltage signals in each case continue to be output in cycles, and the network error-specific digital current and voltage signals are each rebuffered after being output.

German Patent No. 150 947 describes computer-supported testing of protective circuits in which non-stationary processes that are simulated with digital models, for example, are stored and

the stored data is provided to the test object in a specific order. All of the data is accepted before sensing the protective circuit. To test a test object, the data is sent to the test object in a specific order and the signal response of the test object is detected.

One advantage of the method according to the present invention is that it can be carried out with a comparatively simple data processing system design in the form of a conventional personal computer. This is due to the fact that, in the method according to the present application, the digital current and voltage signals output by the data processing system are first buffered consecutively until a specific quantity of buffered digital current and voltage signals is reached. The buffered signals are output in cycles during the test procedure. This applies even if a tripping signal is generated. Nevertheless, the occurrence of the tripping signal causes the data processing system to output network error-specific digital current and voltage signals, which results in a longer computing time than would be needed with an undisturbed, simulated network state, due to the complicated arithmetic operations required. The network error-specific digital current and voltage signals are also buffered. The quantity of digital current and voltage signals is thus replenished. The problem of insufficient computing speed of the relatively simple data processing system used is thus overcome to a certain extent by buffering the signals.

The present invention takes advantage of the fact that, in situations where a protective circuit is used, the tripping signal generated by the circuit when an error occurs in the network to be monitored is immediately applied to a switch, usually a circuit-breaker; however, the circuit-breaker to which this signal is applied does not immediately open its contacts, but instead requires a certain switch response time for this purpose, which ranges between approximately 20 and 100 ms—and is frequently around 60 ms. Only at the end of the

switch response time do new current and voltage ratios actually occur in the network, a fact that must also be taken into account when testing a digital protective circuit with the method according to the present invention.

In light of this fact, it is deemed advantageous in the method according to the present invention to determine the specific quantity of digital current and voltage signals buffered in cycles on the basis of the response time of switches for which the protective circuits to be tested are to be used, taking the cycle time into account. With the method according to the present invention, this ensures that the network error-specific digital current and voltage signals that correspond to the changed network conditions are output at the end of the switch response time, just like in a real situation.

In the method according to the present invention, the buffered digital current and voltage signals can be output at an interval that corresponds to the duration of a tripping signal-free test period needed to output further digital current and voltage signals in each case.

In another embodiment of the method according to the present invention, the buffered digital current and voltage signals are output at an output rate that is greater than the duration of a tripping signal-free test period needed to output digital current and voltage signals in each case.

An arrangement of this type is also described in the publication cited above. To further develop an arrangement of this type so that it can also take into account network error-specific digital current and voltage signals following the generation of a tripping signal, without requiring a great deal of computing power, the data processing system is assigned, according to the present invention, a buffer in which the output digital current and voltage signals are first buffered consecutively; a sensing arrangement that detects

tripping signals from the respective protective circuit is connected on the output side to the data processing system.

The arrangement according to the present invention differs from the arrangement described in German Patent No. 150 947 in that it has a storage device in the form of a buffer in which data is entered during the test and from which data is output during the test. A further difference lies in the provision of a sensing arrangement that controls the data processing system upon the occurrence of a tripping signal from the respective protective circuit to be tested so that the data processing system sends network error-specific data to the buffer.

One significant advantage of the arrangement according to the present invention is that it can make do with a data processing system in the form of a conventional personal computer and can therefore be produced at comparatively little cost; the additional cost of the buffer is comparatively low. A further advantage is that the test can also be carried out with network error-specific current and voltage signals after a tripping signal occurs, using a simple circuitry design.

In the arrangement according to the present invention, the buffer advantageously has a sufficiently large storage capacity to buffer all current and voltage signals output during a tripping signal-free test period corresponding to the response time of switches provided for interaction with the protective circuits to be tested.

The buffer is advantageously a ring buffer, i.e. a buffer in which new data is stored for current and voltage signals previously output by the data processing system.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a block diagram of one example embodiment of the method according to the present invention.

Fig. 2 shows three diagrams illustrating the operation of the buffer shown in the block diagram.

DETAILED DESCRIPTION

Figure 1 shows a block representing a data processing system 1, which is formed by a conventional personal computer. Data processing system 1 includes a network model 2 that can be provided by a NETOMAC simulation program, which is described in detail in the publication mentioned above. Network model 2 outputs digital current and voltage signals J' and U', respectively, via a bus 3, based on the performance of a power supply network to be simulated. These digital current and voltage values J' and U', respectively, are further processed in an interface module 4, which is also used for internal system communication. Interface module 4 is provided with a buffer in the form of a ring buffer 5 in which a specific number of output digital current and voltage signals J' and U', respectively, are buffered. When the test of a digital protective circuit 6 begins, digital current and voltage signals J' and U', respectively, emitted by network model 2 are first buffered in ring buffer 5 in cycles, i.e. based on the system clock. The storage capacity of this ring buffer 5 is selected in view of the system clock cycle so that the buffer becomes full at the end of a period that corresponds to response time Tls of switches (not illustrated) for which protective circuit 6 to be tested is to be used.

When a time Tls of this type elapses after the beginning of the test, a buffered value of current and voltage signal Jz and Uz, respectively, is output from ring buffer 5 with the next system clock cycle and transmitted via a bus 7 to a further interface module 8, which applies a load to a digital-analog converter 10 via an additional bus 9. In this digital-analog converter 10, currents J and voltages U, respectively, corresponding to the respectively transmitted digital current and voltage values are generated and supplied to protective circuit 6 to be tested via amplifiers 11 and 12. Diagram A of

Figure 2 shows the variation over time t of voltage U generated in this manner. Likewise, Diagram B shows generated current J over time, which initially appears to have a value of zero only due to the scale selected. Diagram C of Figure 2 shows number n of the digital current and voltage values stored in ring buffer 5 over time t. Prior to a time T1 after the beginning of the test, only ring buffer 5 is first filled with digital current and voltage values at time zero. After time T1 is reached, the amount of data entered into the ring buffer cyclically equals the amount of data output. This means that number n of stored data remains the same after time T1.

In the illustrated example, it is assumed that protective circuit 6 to be tested emits a tripping signal S at time T2 as a result of current and voltage values J and U that it receives. This tripping signal S is detected by a sensing arrangement 13 and passed on to the one interface module 4 via a further interface module 8 over a bus 14. The one interface module 4 subsequently causes network model 2 to output, via a bus 15, digital current and voltage signals that are network error-specific, i.e. would occur in the event of a short-circuit in the simulated network. As shown in Diagrams A and B of Figure 2, fluctuations occur over a period ΔT, the calculation of which in network model 2 requires a relatively large amount of computing power and thus takes a relatively long time so that these network error-specific digital current and voltage signals are output at a relatively slow rate. Because the buffered digital current and voltage values continue to be output from ring buffer 5 in cycles, although not at the same rate at which network error-specific digital current and voltage values are generated by network model 2, the quantity of buffered data in ring buffer 5 starts to decrease from time T2 onward, as clearly illustrated by Diagram C of Figure 2.

If it is assumed that digital current and voltage signals J' and U' in the network model are output at an interval Δt that

is equal to required computing time tmin when a tripping signal S is not present and a fluctuation does not occur, ring buffer 5 cannot be completely refilled. However, if it is assumed that the computing time of network model 2 is tmax after a tripping signal occurs, fluctuations can occur in response time Tls of the switches during a simulation Tls/(tmax-tmin) until the buffer is empty. Assuming typical values for tmax=1 ms, tmin=0.5 ms, and Tls=60 ms, 120 fluctuations can occur during the simulation until ring buffer 5 can no longer provide any more output data. In practice, this is entirely sufficient.

In the illustrated example, it is assumed that interval Δt is greater than required computing time tmin of network model 2 before a tripping signal S occurs, and that $\Delta t > tmin$. Filling time tf of ring buffer 5 can then be determined with the following equation:

$$tf = \left(\frac{t\max - F \cdot t\min}{F - 1} \right) \cdot F$$

where $F=\Delta t/tmin$. The assumptions described above by way of an example then yield a filling time tf of roughly 5 ms. This means that simulations lasting 5 ms without any fluctuations are sufficient to compensate for the time lost by the fluctuation calculation and to completely refill ring buffer 5. This gives the system a 90% increase in performance in this case. As clearly shown by Figure C, simulations of practically unlimited length can be carried out in this case because the switch never carries out a sufficiently large number of switching operations in a short period of time to allow buffer 5 to be emptied.

Abstract

A method and an arrangement for testing digital protective circuits in which data processing means are used to simulate a power supply network by outputting digital current and voltage signals in cycles. Corresponding current and voltages are generated from these signals and supplied to a protective circuit to be tested. To test protective circuits under conditions that are as close to reality as possible with a method of this type, using a comparatively simple data processing system design, the output digital current and voltage signals are first buffered consecutively when the test of a protective circuit begins. Upon reaching a specific quantity of buffered signals, the oldest buffered signals in each case are output in cycles, and more recent output signals are buffered. Upon the occurrence of a tripping signal, output continues in cycles, and data processing means output and buffer network-specific digital current and voltage signals.

[67190/978621]

METHOD AND ARRANGEMENT FOR TESTING DIGITAL PROTECTIVE CIRCUITS

[Description] **FIELD OF THE INVENTION**

The present invention relates to a method for testing digital protective circuits in which data processing means are used to simulate the current and voltage response of a power supply network by outputting digital current and voltage signals in cycles; corresponding currents and voltages are generated from the digital current and voltage signals and supplied to a protective circuit to be tested; and tripping signals from the respective protective circuit are detected.

BACKGROUND INFORMATION

A method of this type is [generally known from] **described in** "Elektrizitätswirtschaft", Vol. 78 (1979), No. 1, pages 18 to 23. [According to a] **In this** method [of this type], a data processing system emits digital current and voltage signals in cycles on the basis of the current and voltage ratios present in a power supply network; the data processing system thus forms a network model. Corresponding currents and voltages can be generated from the digital current and voltage signals and supplied to a protective circuit to be tested. When currents and voltages corresponding to an error in the simulated power supply network are applied to the protective circuit to be tested, the latter generates a tripping signal. The occurrence of the tripping signal can be assigned to the respective currents and voltages to draw conclusions about the tripping performance of the respective protective circuit to be tested.

To test the digital protective circuits under conditions that are as close to reality as possible, it is useful to control the data processing system simulating the power supply network and representing a network model when detecting a tripping signal so that the data processing system also outputs network error-specific digital current and voltage signals. Because

this requires longer computing times than are needed for digital current and voltage signals that indicate a normal, continuous variation of currents and voltages, it is [conceivable] **possible** to use a very high-speed data processing system and to have the latter output network error-specific digital current and voltage signals when a tripping signal is emitted by the respective protective circuit to be tested. However, a data processing system of this type is highly complex and therefore very expensive to produce or purchase.

SUMMARY

An [The] object of the present invention is to provide a method for testing digital protective circuits in which a conventional data processing system, such as a personal computer, can be used to test digital protective circuits under close-to-real conditions even using network error-specific digital current and voltage signals from a data processing system of this type.

This object is achieved with a method according to the present invention [of the type mentioned in the preamble] in that when the test of a protective circuit begins, the output digital current and voltage signals are first buffered consecutively, and, upon reaching a specific quantity of buffered digital current and voltage signals, the oldest buffered digital current and voltage signals in each case are output in cycles and supplied to the respective protective circuit to be tested, and more recent output digital current and voltage signals are rebuffered; upon the occurrence of a tripping signal, **a** data processing [means output] **arrangement outputs** network error-specific digital current and voltage signals, while the oldest buffered digital current and voltage signals in each case continue to be output in cycles, and the network error-specific digital current and voltage signals are each rebuffered after being output.

German Patent No. 150 947 describes computer-supported testing of protective circuits in which non-stationary processes that are simulated with digital models, for example, are stored and the stored data is provided to the test object in a specific order. All of the data is accepted before sensing the protective circuit. To test a test object, the data is sent to the test object in a specific order and the signal response of the test object is detected.

One [A significant] advantage of the method according to the present invention is that it can be carried out with a comparatively simple data processing system design in the form of a conventional personal computer. This is due to the fact that, in the method according to the present application, the digital current and voltage signals output by the data processing system are first buffered consecutively until a specific quantity of buffered digital current and voltage signals is reached. The buffered signals are output in cycles during the test procedure. This applies even if a tripping signal is generated. Nevertheless, the occurrence of the tripping signal causes the data processing system to output network error-specific digital current and voltage signals, which results in a longer computing time than would be needed with an undisturbed, simulated network state, due to the complicated arithmetic operations required. The network error-specific digital current and voltage signals are also buffered. The quantity of digital current and voltage signals is thus replenished. The problem of [essentially] insufficient computing speed of the relatively simple data processing system used is thus overcome to a certain extent by buffering the signals.

The present invention takes advantage of the fact that, in situations where a protective circuit is used, the tripping signal generated by the circuit when an error occurs in the network to be monitored is immediately applied to a switch,

usually a circuit-breaker; however, the circuit-breaker to which this signal is applied does not immediately open its contacts, but instead requires a certain switch response time for this purpose, which ranges between approximately 20 and 100 ms—and is frequently around 60 ms. Only at the end of the switch response time do new current and voltage ratios actually occur in the network, a fact that must also be taken into account when testing a digital protective circuit with the method according to the present invention.

In light of this fact, it is deemed advantageous in the method according to the present invention to determine the specific quantity of digital current and voltage signals buffered in cycles on the basis of the response time of switches for which the protective circuits to be tested are to be used, taking the cycle time into account. With the method according to the present invention, this ensures that the network error-specific digital current and voltage signals that correspond to the changed network conditions are output at the end of the switch response time, just like in a real situation.

In the method according to the present invention, the buffered digital current and voltage signals can be output at [a variable output rate. It is viewed as advantageous to output the buffered] **an interval that corresponds to the duration of a tripping signal-free test period needed to output further** digital current and voltage signals [at an output rate that corresponds to the duration of a tripping signal-free test period needed to output further digital current and voltage signals] in each case[, thus achieving cyclical output. While the quantity of buffered current and voltage signals in a method of this type is used up after a certain amount of time following a simulated network error, it frequently is fully sufficient for a practical simulation. The special advantage is that, in this embodiment of the method according to the

present invention, the output frequency of the digital current and voltage signals can be more or less doubled compared to the method described in the preamble].

In another embodiment of the method according to the present invention, the buffered digital current and voltage signals are output at an output rate that is greater than the duration of a tripping signal-free test period needed to output digital current and voltage signals[. In this embodiment of the method according to the present invention, the quantity of buffered digital current and voltage signals is replenished after a tripping signal occurs so that, according to this method embodiment, simulations of practically any duration can be carried out.

The present invention also concerns a test arrangement including a data processing system that simulates the current and voltage response of a power supply network in the form of a network model by outputting digital current and voltage signals in cycles, and including a converter unit, located downstream from the data processing system, which generates corresponding currents and voltages from the digital current and voltage signals and supplies them to a protective circuit to be tested.] **in each case.**

An arrangement of this type is also [generally known from] **described in** the publication cited above. To further develop an arrangement of this type so that it can also take into account network error-specific digital current and voltage signals following the generation of a tripping signal, without requiring a great deal of computing power, the data processing system is assigned, according to the present invention, a buffer in which the output digital current and voltage signals are first buffered consecutively; a sensing arrangement that detects tripping signals from the respective protective

circuit is connected on the output side to the data processing system.

The arrangement according to the present invention differs from the arrangement described in German Patent No. 150 947 in that it has a storage device in the form of a buffer in which data is entered during the test and from which data is output during the test. A further difference lies in the provision of a sensing arrangement that controls the data processing system upon the occurrence of a tripping signal from the respective protective circuit to be tested so that the data processing system sends network error-specific data to the buffer.

One significant advantage of the arrangement according to the present invention is that it can make do with a data processing system in the form of a conventional personal computer and can therefore be produced at comparatively little cost; the additional cost of the buffer is comparatively low. A further advantage is that the test can also be carried out with network error-specific current and voltage signals after a tripping signal occurs, using a simple circuitry design.

In the arrangement according to the present invention, the buffer advantageously has a sufficiently large storage capacity to buffer all current and voltage signals output during a tripping signal-free test period corresponding to the response time of switches provided for interaction with the protective circuits to be tested.

The buffer is advantageously a ring buffer, i.e. a buffer in which new data is stored for current and voltage signals previously output by the data processing system.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. [To further explain the present invention, Figure] 1 shows a block diagram [illustrating] **of** one **example** embodiment of the method according to the present invention[, while Figure].

Fig. 2 shows three diagrams illustrating the operation of the buffer shown in the block diagram.

DETAILED DESCRIPTION

Figure 1 shows a block representing a data processing system 1, which is formed by a conventional personal computer. Data processing system 1 includes a network model 2 that can be provided by a NETOMAC simulation program, which is described in detail in the publication mentioned [in the preamble] **above**. Network model 2 outputs digital current and voltage signals J' and U', respectively, via a bus 3, based on the performance of a power supply network to be simulated. These digital current and voltage values [I'] **J'** and U', respectively, are further processed in an interface module 4, which is also used for internal system communication. Interface module 4 is provided with a buffer in the form of a ring buffer 5 in which a specific number of output digital current and voltage signals J' and U', respectively, are buffered. When the test of a digital protective circuit 6 begins, digital current and voltage signals J' and U', respectively, emitted by network model 2 are first buffered in ring buffer 5 in cycles, i.e. based on the system clock. The storage capacity of this ring buffer 5 is selected in view of the system clock cycle so that the buffer becomes full at the end of a period that corresponds to response time Tls of switches (not illustrated) for which protective circuit 6 to be tested is to be used.

When a time Tls of this type elapses after the beginning of the test, a buffered value of current and voltage signal Jz and Uz, respectively, is output from ring buffer 5 with the next system clock cycle and transmitted via a bus 7 to a

further interface module 8, which applies a load to a digital-analog converter 10 via an additional bus 9. In this digital-analog converter 10, currents J and voltages U, respectively, corresponding to the respectively transmitted digital current and voltage values are generated and supplied to protective circuit 6 to be tested via amplifiers 11 and 12. Diagram A of Figure 2 shows the variation over time t of voltage U generated in this manner. Likewise, Diagram B shows generated current J over time, which initially appears to have a value of zero only due to the scale selected. Diagram C of Figure 2 shows number n of the digital current and voltage values stored in ring buffer 5 over time t. [We can see that, prior] **Prior** to a time T1 after the beginning of the test, only ring buffer 5 is first filled with digital current and voltage values at time zero. After time T1 is reached, the amount of data entered into the ring buffer cyclically equals the amount of data output. This means that number n of stored data remains the same after time T1.

In the illustrated example, it is assumed that protective circuit 6 to be tested emits a tripping signal S at time T2 as a result of current and voltage values J and U that it receives. This tripping signal S is detected by a sensing arrangement 13 and passed on to the one interface module 4 via a further interface module 8 over a bus 14. The one interface module 4 subsequently causes network model 2 to output, via a bus 15, digital current and voltage signals that are network error-specific, i.e. would occur in the event of a short-circuit in the simulated network. As shown in Diagrams A and B of Figure 2, fluctuations occur over a period ΔT, the calculation of which in network model 2 requires a relatively large amount of computing power and thus takes a relatively long time so that these network error-specific digital current and voltage signals are output at a relatively slow rate. Because the buffered digital current and voltage values continue to be output from ring buffer 5 in cycles, although

not at the same rate at which network error-specific digital current and voltage values are generated by network model 2, the quantity of buffered data in ring buffer 5 starts to decrease from time T2 onward, as clearly illustrated by Diagram C of Figure 2.

If [we assume] **it is assumed** that [output rate Δt of] digital current and voltage signals J' and U' in the network model **are output at an interval Δt that** is equal to required computing time tmin when a tripping signal S is not present and a fluctuation does not occur, ring buffer 5 cannot be completely refilled. However, if [we assume] **it is assumed** that the computing time of network model 2 is tmax after a tripping signal occurs, fluctuations can occur in response time Tls of the switches during a simulation Tls/(tmax-tmin) until the buffer is empty. Assuming typical values for tmax=1 ms, tmin=0.5 ms, and Tls=60 ms, 120 fluctuations can occur during the simulation until ring buffer 5 can no longer provide any more output data. In practice, this is entirely sufficient.

In the illustrated example, it is assumed that [output rate] **interval** Δt is greater than required computing time tmin of network model 2 before a tripping signal S occurs, and that Δt>tmin. Filling time tf of ring buffer 5 can then be determined with the following equation:

$$tf = \left(\frac{t\max - F \cdot t\min}{F - 1} \right) \cdot F$$

where F=Δt/tmin. The assumptions described above by way of an example then yield a filling time tf of roughly 5 ms. This means that simulations lasting 5 ms without any fluctuations are sufficient to compensate for the time lost by the fluctuation calculation and to completely refill ring buffer

5. This gives the system a 90% increase in performance in this case. As clearly shown by Figure C, simulations of practically unlimited length can be carried out in this case because the switch never carries out a sufficiently large number of switching operations in a short period of time to allow buffer 5 to be emptied.

Abstract

A method and an arrangement for testing digital protective circuits in which data processing means are used to simulate a power supply network by outputting digital current and voltage signals in cycles. Corresponding current and voltages are generated from these signals and supplied to a protective circuit to be tested. [
]To test protective circuits under conditions that are as close to reality as possible with a method of this type, using a comparatively simple data processing system design, the output digital current and voltage signals [(J', U')] are first buffered consecutively when the test of a protective circuit [(6)] begins. Upon reaching a specific quantity of buffered signals[(Iz, Uz)], the oldest buffered signals [(Iz, Uz)] in each case are output in cycles, and more recent output signals [(J', U')] are buffered. Upon the occurrence of a tripping signal, output continues in cycles, and data processing means output and buffer network-specific digital current and voltage signals.
[
FIG 1]

[67190/978621]

METHOD AND ARRANGEMENT FOR TESTING DIGITAL PROTECTIVE CIRCUITS

Description

The present invention relates to a method for testing digital protective circuits in which data processing means are used to simulate the current and voltage response of a power supply network by outputting digital current and voltage signals in cycles; corresponding currents and voltages are generated from the digital current and voltage signals and supplied to a protective circuit to be tested; and tripping signals from the respective protective circuit are detected.

A method of this type is generally known from "Elektrizitätswirtschaft", Vol. 78 (1979), No. 1, pages 18 to 23. According to a method of this type, a data processing system emits digital current and voltage signals in cycles on the basis of the current and voltage ratios present in a power supply network; the data processing system thus forms a network model. Corresponding currents and voltages can be generated from the digital current and voltage signals and supplied to a protective circuit to be tested. When currents and voltages corresponding to an error in the simulated power supply network are applied to the protective circuit to be tested, the latter generates a tripping signal. The occurrence of the tripping signal can be assigned to the respective currents and voltages to draw conclusions about the tripping performance of the respective protective circuit to be tested.

To test the digital protective circuits under conditions that are as close to reality as possible, it is useful to control the data processing system simulating the power supply network and representing a network model when detecting a tripping signal so that the data processing system also outputs network error-specific digital current and voltage signals. Because this requires longer computing times than are needed for digital current and voltage signals that indicate a normal,

continuous variation of currents and voltages, it is conceivable to use a very high-speed data processing system and to have the latter output network error-specific digital current and voltage signals when a tripping signal is emitted by the respective protective circuit to be tested. However, a data processing system of this type is highly complex and therefore very expensive to produce or purchase.

The object of the present invention is to provide a method for testing digital protective circuits in which a conventional data processing system, such as a personal computer, can be used to test digital protective circuits under close-to-real conditions even using network error-specific digital current and voltage signals from a data processing system of this type.

This object is achieved with a method according to the present invention of the type mentioned in the preamble in that when the test of a protective circuit begins, the output digital current and voltage signals are first buffered consecutively, and, upon reaching a specific quantity of buffered digital current and voltage signals, the oldest buffered digital current and voltage signals in each case are output in cycles and supplied to the respective protective circuit to be tested, and more recent output digital current and voltage signals are rebuffered; upon the occurrence of a tripping signal, data processing means output network error-specific digital current and voltage signals, while the oldest buffered digital current and voltage signals in each case continue to be output in cycles, and the network error-specific digital current and voltage signals are each rebuffered after being output.

A significant advantage of the method according to the present invention is that it can be carried out with a comparatively simple data processing system design in the form of a conventional personal computer. This is due to the fact that,

in the method according to the present application, the digital current and voltage signals output by the data processing system are first buffered consecutively until a specific quantity of buffered digital current and voltage signals is reached. The buffered signals are output in cycles during the test procedure. This applies even if a tripping signal is generated. Nevertheless, the occurrence of the tripping signal causes the data processing system to output network error-specific digital current and voltage signals, which results in a longer computing time than would be needed with an undisturbed, simulated network state, due to the complicated arithmetic operations required. The network error-specific digital current and voltage signals are also buffered. The quantity of digital current and voltage signals is thus replenished. The problem of essentially insufficient computing speed of the relatively simple data processing system used is thus overcome to a certain extent by buffering the signals.

The present invention takes advantage of the fact that, in situations where a protective circuit is used, the tripping signal generated by the circuit when an error occurs in the network to be monitored is immediately applied to a switch, usually a circuit-breaker; however, the circuit-breaker to which this signal is applied does not immediately open its contacts, but instead requires a certain switch response time for this purpose, which ranges between approximately 20 and 100 ms—and is frequently around 60 ms. Only at the end of the switch response time do new current and voltage ratios actually occur in the network, a fact that must also be taken into account when testing a digital protective circuit with the method according to the present invention.

In light of this fact, it is deemed advantageous in the method according to the present invention to determine the specific quantity of digital current and voltage signals buffered in cycles on the basis of the response time of switches for which

the protective circuits to be tested are to be used, taking the cycle time into account. With the method according to the present invention, this ensures that the network error-specific digital current and voltage signals that correspond to the changed network conditions are output at the end of the switch response time, just like in a real situation.

In the method according to the present invention, the buffered digital current and voltage signals can be output at a variable output rate. It is viewed as advantageous to output the buffered digital current and voltage signals at an output rate that corresponds to the duration of a tripping signal-free test period needed to output further digital current and voltage signals in each case, thus achieving cyclical output. While the quantity of buffered current and voltage signals in a method of this type is used up after a certain amount of time following a simulated network error, it frequently is fully sufficient for a practical simulation. The special advantage is that, in this embodiment of the method according to the present invention, the output frequency of the digital current and voltage signals can be more or less doubled compared to the method described in the preamble.

In another embodiment of the method according to the present invention, the buffered digital current and voltage signals are output at an output rate that is greater than the duration of a tripping signal-free test period needed to output digital current and voltage signals. In this embodiment of the method according to the present invention, the quantity of buffered digital current and voltage signals is replenished after a tripping signal occurs so that, according to this method embodiment, simulations of practically any duration can be carried out.

The present invention also concerns a test arrangement including a data processing system that simulates the current and voltage response of a power supply network in the form of

a network model by outputting digital current and voltage signals in cycles, and including a converter unit, located downstream from the data processing system, which generates corresponding currents and voltages from the digital current and voltage signals and supplies them to a protective circuit to be tested.

An arrangement of this type is also generally known from the publication cited above. To further develop an arrangement of this type so that it can also take into account network error-specific digital current and voltage signals following the generation of a tripping signal, without requiring a great deal of computing power, the data processing system is assigned, according to the present invention, a buffer in which the output digital current and voltage signals are first buffered consecutively; a sensing arrangement that detects tripping signals from the respective protective circuit is connected on the output side to the data processing system.

One significant advantage of the arrangement according to the present invention is that it can make do with a data processing system in the form of a conventional personal computer and can therefore be produced at comparatively little cost; the additional cost of the buffer is comparatively low. A further advantage is that the test can also be carried out with network error-specific current and voltage signals after a tripping signal occurs, using a simple circuitry design.

In the arrangement according to the present invention, the buffer advantageously has a sufficiently large storage capacity to buffer all current and voltage signals output during a tripping signal-free test period corresponding to the response time of switches provided for interaction with the protective circuits to be tested.

The buffer is advantageously a ring buffer, i.e. a buffer in which new data is stored for current and voltage signals previously output by the data processing system.

To further explain the present invention, Figure 1 shows a block diagram illustrating one embodiment of the method according to the present invention, while Figure 2 shows three diagrams illustrating the operation of the buffer shown in the block diagram.

Figure 1 shows a block representing a data processing system 1, which is formed by a conventional personal computer. Data processing system 1 includes a network model 2 that can be provided by a NETOMAC simulation program, which is described in detail in the publication mentioned in the preamble. Network model 2 outputs digital current and voltage signals J' and U', respectively, via a bus 3, based on the performance of a power supply network to be simulated. These digital current and voltage values I' and U', respectively, are further processed in an interface module 4, which is also used for internal system communication. Interface module 4 is provided with a buffer in the form of a ring buffer 5 in which a specific number of output digital current and voltage signals J' and U', respectively, are buffered. When the test of a digital protective circuit 6 begins, digital current and voltage signals J' and U', respectively, emitted by network model 2 are first buffered in ring buffer 5 in cycles, i.e. based on the system clock. The storage capacity of this ring buffer 5 is selected in view of the system clock cycle so that the buffer becomes full at the end of a period that corresponds to response time Tls of switches (not illustrated) for which protective circuit 6 to be tested is to be used.

When a time Tls of this type elapses after the beginning of the test, a buffered value of current and voltage signal Jz and Uz, respectively, is output from ring buffer 5 with the next system clock cycle and transmitted via a bus 7 to a

further interface module 8, which applies a load to a digital-analog converter 10 via an additional bus 9. In this digital-analog converter 10, currents J and voltages U, respectively, corresponding to the respectively transmitted digital current and voltage values are generated and supplied to protective circuit 6 to be tested via amplifiers 11 and 12. Diagram A of Figure 2 shows the variation over time t of voltage U generated in this manner. Likewise, Diagram B shows generated current J over time, which initially appears to have a value of zero only due to the scale selected. Diagram C of Figure 2 shows number n of the digital current and voltage values stored in ring buffer 5 over time t. We can see that, prior to a time T1 after the beginning of the test, only ring buffer 5 is first filled with digital current and voltage values at time zero. After time T1 is reached, the amount of data entered into the ring buffer cyclically equals the amount of data output. This means that number n of stored data remains the same after time T1.

In the illustrated example, it is assumed that protective circuit 6 to be tested emits a tripping signal S at time T2 as a result of current and voltage values J and U that it receives. This tripping signal S is detected by a sensing arrangement 13 and passed on to the one interface module 4 via a further interface module 8 over a bus 14. The one interface module 4 subsequently causes network model 2 to output, via a bus 15, digital current and voltage signals that are network error-specific, i.e. would occur in the event of a short-circuit in the simulated network. As shown in Diagrams A and B of Figure 2, fluctuations occur over a period ΔT, the calculation of which in network model 2 requires a relatively large amount of computing power and thus takes a relatively long time so that these network error-specific digital current and voltage signals are output at a relatively slow rate. Because the buffered digital current and voltage values continue to be output from ring buffer 5 in cycles, although

not at the same rate at which network error-specific digital current and voltage values are generated by network model 2, the quantity of buffered data in ring buffer 5 starts to decrease from time T2 onward, as clearly illustrated by Diagram C of Figure 2.

If we assume that output rate Δt of digital current and voltage signals J' and U' in the network model is equal to required computing time tmin when a tripping signal S is not present and a fluctuation does not occur, ring buffer 5 cannot be completely refilled. However, if we assume that the computing time of network model 2 is tmax after a tripping signal occurs, fluctuations can occur in response time Tls of the switches during a simulation Tls/(tmax-tmin) until the buffer is empty. Assuming typical values for tmax=1 ms, tmin=0.5 ms, and Tls=60 ms, 120 fluctuations can occur during the simulation until ring buffer 5 can no longer provide any more output data. In practice, this is entirely sufficient.

In the illustrated example, it is assumed that output rate Δt is greater than required computing time tmin of network model 2 before a tripping signal S occurs, and that $\Delta t > tmin$. Filling time tf of ring buffer 5 can then be determined with the following equation:

$$tf = \left(\frac{t\max - F \cdot t\min}{F - 1} \right) \cdot F$$

where $F=\Delta t/tmin$. The assumptions described above by way of an example then yield a filling time tf of roughly 5 ms. This means that simulations lasting 5 ms without any fluctuations are sufficient to compensate for the time lost by the fluctuation calculation and to completely refill ring buffer 5. This gives the system a 90% increase in performance in this case. As clearly shown by Figure C, simulations of practically

unlimited length can be carried out in this case because the switch never carries out a sufficiently large number of switching operations in a short period of time to allow buffer 5 to be emptied.

Patent Claims

1. A method for testing digital protective circuits in which
- data processing means are used to simulate the current and voltage response of a power supply network by outputting digital current and voltage signals (J', U') in cycles;
- corresponding currents (J) and voltages (U) are generated from the digital current and voltage signals (J', U') and supplied to a protective circuit (6) to be tested; and
- tripping signals (S) from the respective protective circuit (6) are detected,

characterized in that
- when the test of a protective circuit (6) begins, the output digital current and voltage signals (J', U') are first buffered consecutively;
- upon reaching a specific quantity of buffered digital current and voltage signals (Jz, Uz), the oldest buffered digital current and voltage signals (Jz, Uz) in each case are output in cycles and supplied to the respective protective circuit (6) to be tested, and more recent output digital current and voltage signals (J', U') are rebuffered; and
- upon the occurrence of a tripping signal (S), data processing means output network error-specific digital current and voltage signals (J', U'), while the oldest buffered digital current and voltage signals (Jz, Uz) in each case continue to be output in cycles, and the network error-specific digital current and voltage signals (J', U') are each buffered after being output.

2. The method according to Claim 1,
characterized in that
- the specific quantity of digital current and voltage signals (Jz, Uz) buffered in cycles is determined on the basis of the response time (Tls) of switches for which the protective circuits (6) to be tested are to be used, taking the cycle time into account.

3. The method according to Claim 1 or 2,
characterized in that

- the buffered digital current and voltage signals (Iz, Uz) are output at an output rate (Δt) that corresponds to the duration of a tripping signal-free test period needed to output further digital current and voltage signals (J', U') in each case.

4. The method according to Claim 1 or 2,
characterized in that

- the buffered digital current and voltage signals (Jz, Uz) are output at an output rate (Δt) that is greater than the duration of a tripping signal-free test period needed to output further digital current and voltage signals (J', U') in each case.

5. An arrangement for testing digital protective circuits,
having

- a data processing system (1) that simulates the current and voltage response of a power supply network in the form of a network model by outputting digital current and voltage signals (J', U') in cycles; and
- a converter unit (10), located downstream from the data processing system (1), which generates corresponding currents and voltages (J, U) from the digital current and voltage signals (J', U') and supplies them to a protective circuit (6) to be tested,

characterized in that

- the data processing system (1) is assigned a buffer (5) in which the output digital current and voltage signals (J', U') are first buffered consecutively; and
- a sensing arrangement (13) that detects tripping signals (S) from the respective protective circuit (6) is connected on the output side to the data processing system (1).

6. The arrangement according to Claim 5,
characterized in that

- the buffer (5) has a sufficiently large storage capacity to buffer all current and voltage signals (J', U') output during a tripping signal-free test period corresponding to the response time (Tls) of switches provided for interaction with the protective circuits (6) to be tested.

7. The arrangement according to Claim 5 or 6, characterized in that

- the buffer is a ring buffer (5).

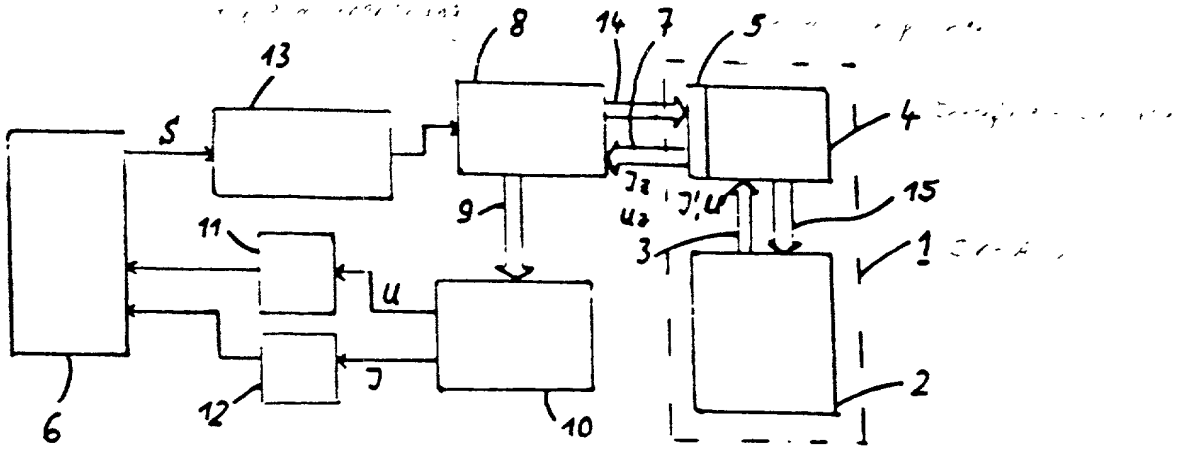


Fig 1

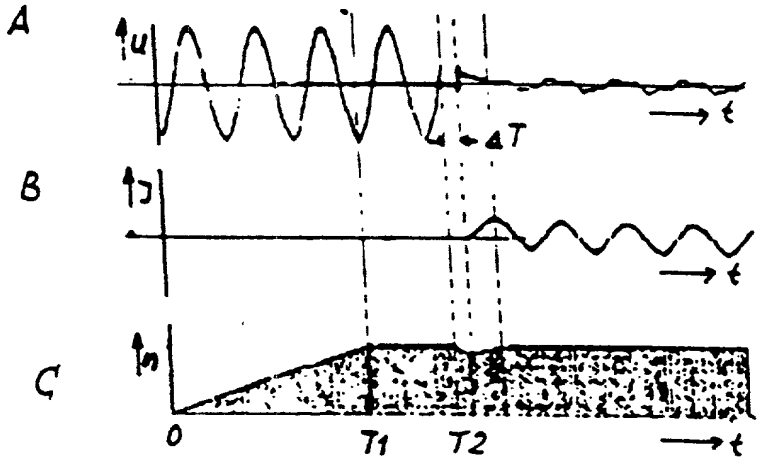


Fig 2

[67190/978621]

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **METHOD AND ARRANGEMENT FOR TESTING DIGITAL PROTECTIVE CIRCUITS**, the specification for which was filed in the United States Patent and Trademark Office on March 10, 2000, Serial No. 09/508,396.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

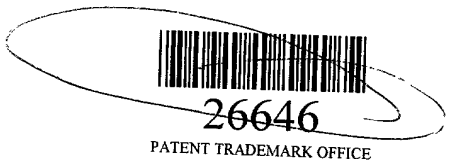
Number	Country filed	Day/month/year	Priority Claimed Under 35 USC 119
197 40 425.1	Fed. Rep. of Germany	10 September 1997	Yes

EL 244506391 US

And I hereby appoint Richard L. Mayer (Reg. No. 22,490), Gerard A. Messina (Reg. No. 35,952) and Michelle Carniaux (Reg. No. 36,098) as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Please address all communications regarding this application to:

KENYON & KENYON
One Broadway
New York, New York 10004



Please direct all telephone calls to Richard L. Mayer at (212) 425-7200.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful and false statements may jeopardize the validity of the application or any patent issued thereon.

Inventor: 1-00 **Steffen KAISER**

Inventor's Signature: Steffen Kaiser

Date: 08.07.01

Residence: Dimitroffstr. 123
10407 Berlin, DE
Federal Republic of Germany

Citizenship: Federal Republic of Germany

Post Office Address: Same as above.

Inventor: 2-10 **Wilhelm WINTER**

Inventor's Signature: _____

Date: 4.2.01

Residence: Eichenweg 10
91054 Erlangen DEX
Federal Republic of Germany

Citizenship: Federal Republic of Germany

Post Office Address: Same as above.

287990